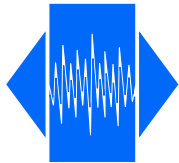


VTX5S

High reliable, accurate,
analogue temperature compensated (VC)TCXO

Generic specification

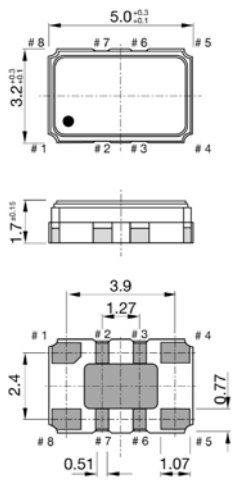
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Frequency range	5.0000 ~ 60.0000 MHz		
Standard frequencies (fundamental)	5, 10, 12, 12.8, 13, 14.4, 16, 16.384, 16.36766, 19.2, 19.44, 20, 24, 25, 26, 32, 32.768, 38.88, 40, 50, 60(Δ) MHz		
Frequency stability:			
vs. temperature referenced to $(F_{MAX}+F_{MIN})/2$	$\leq \pm 0.50$ ppm	over -40 to +85 °C	(*)
vs. supply voltage changes referenced to frequency at nominal supply	$\leq \pm 0.1$ ppm	± 5 %	
vs. load changes referenced to frequency at nominal load	$\leq \pm 0.1$ ppm	± 5 %	
vs. aging @ +40 °C	$\leq \pm 1.0$ ppm	1 st year	
G-sensitivity	< 2.0 ppb/g	per axis	
Frequency tolerance ex. factory	0 ~ +1.0 ppm	@ +25 °C	
Supply voltage	+2.5 V, +3.0 V or +3.3 V		(*)
Output signal	Clipped sine wave	CMOS	(*)
Output level	> 0.8 Vp-p	$V_{OH} > 0.9*V_{CC} / V_{OL} < 0.1*V_{CC}$	
Output load	10 kΩ // 10 pF	15 pF Max.	
Current consumption, depending on frequency	5 < mA	< 8 mA	
Electronic Frequency Control (EFC)	$\Delta F = \pm 5$ to ± 10 ppm	positive slope	(*)
Control voltage (Vc)	+1.50 V ± 1.0 V		(*)
EFC input impedance	> 100 kΩ		
Tri-state function	pin #6 → high or open pin #6 → low or GND	pin #5 → oscillation pin #5 → high impedance	
Phase noise (typical value for 40 MHz)	LN (Low phase noise)	Standard	Frequency offset
	-85 dBc/Hz -115 dBc/Hz -138 dBc/Hz -150 dBc/Hz -154 dBc/Hz	-83 dBc/Hz -110 dBc/Hz -135 dBc/Hz -148 dBc/Hz -152 dBc/Hz	@ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz @ 100 kHz
Operating temperature range	-40 ~ +85 °C		(*)
Storage temperature range	-55 ~ +105 °C		
Reflow Profiles as per IPC/JEDEC J-STD-020C	≤ 260 °C over 10 sec. Max.		
Moisture sensitivity	Level 1 (unlimited)		

(*) See available options on page #2

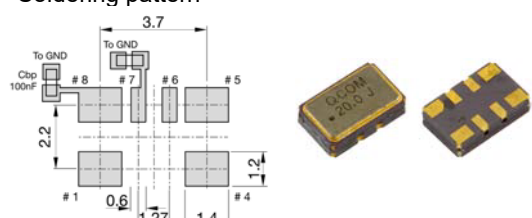
Note: Unless otherwise specified conditions are @+25 °C



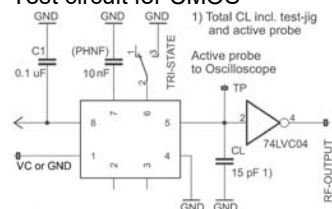
Pin function

- # 1 Vc (EFC) for VC-TCXO
GND or NC for TCXO
- # 2 do not connect
- # 3 do not connect
- # 4 GND
- # 5 OUTPUT
- # 6 Tri-state or do not connect
- # 7 LN: 10 nF to the GND
or do not connect
- # 8 Vcc

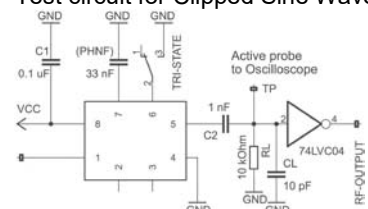
Soldering pattern



Test circuit for CMOS



Test circuit for Clipped Sine Wave



2011/65/EU RoHS compliant

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From design to production
in Switzerland

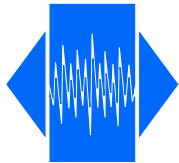


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VTX5S

High reliable, accurate,
analogue temperature compensated (VC)TCXO

QuartzCom
the communications company



Generic specification

Ordering code

(0)5S-(1)(2)-(3)(4)-(5)(7)-40.000MHz Example: **VT5S-C33-NNu50-V05LN-40.000MHz**

(0) Oscillator type	(1) Output signal	(2) Supply voltage	(7) Phase noise option
TX = TCXO VT = VC-TCXO	H = CMOS C = Clipped sine wave	25 = 2.5 V 30 = 3.0 V 33 = 3.3 V	LN = Low phase noise (-) = Standard
(3) Operating temperature	(4) Frequency stability	(5) Pulling range (VT only)	
JF = -20 to +50 °C JK = -20 to +70 °C NN = -40 to +85 °C NR = -40 to +105 °C QN = -55 to +85 °C	u25 = ± 0.25 ppm u50 = ± 0.50 ppm 1u0 = ± 1.00 ppm 1u5 = ± 1.50 ppm	V05 = 1.5 ± 1.0 V ±5 ppm V10 = 1.5 ± 1.0 V ±10 ppm Z = special spec	

Frequency stability vs. temperature

ppm	≤± 0.20	≤± 0.25	≤± 0.50	≤± 1.00	≤± 1.50
-20 to +50 °C	O	O	O	O	O
-20 to +70 °C	Δ	O	O	O	O
-40 to +85 °C	Δ	Δ	O	O	O
-40 to +95 °C	X	Δ	Δ	Δ	O
-40 to +105 °C	X	X	X	Δ	Δ
-55 to +85 °C	X	X	X	X	Δ

Δ Ask factory
O Available
X Not available

Environmental conditions

Test	IEC 60068 Part...	IEC 60679-1 Clause	MIL-STD-202G Method	MIL-STD-810F Method	MIL-PRF-55310D Clause	Test conditions (IEC)
Sealing tests (if applicable)	2-17	5.6.2	112E		3.6.1.2	Gross leak: Test Qc, Fine leak: Test Qk
Solderability Resistance to soldering heat	2-20 2-58	5.6.3	208H 210F		3.6.52 3.6.48	Test Ta method 1, Test Td ₁ method 2, Test Td ₂ method 2
Shock *	2-27	5.6.8	213B Cond C	516.4	3.6.40	Test Ea, 3 x per axis 100 g, 6 ms half-sine pulse
Vibration, sinusoidal*	2-6	5.6.7.1	204D Cond A	516.4-4	3.6.38.1 3.6.38.2	Test Fc, 30 min per axis, 10 Hz – 55 Hz 0,75 mm; 55 Hz – 2 kHz, 10 g
Vibration, random*	2-64	5.6.7.3	214A	514.5	3.6.38.3 3.6.38.4	Test Fdb
Endurance tests - ageing - extended ageing		5.7.1 5.7.2	108A		4.8.35	30 days @ 85 °C 1000 h, 2000 h, 8000 h @ 85 °C

Other environmental conditions on request

28 Dec. 20

2011/65/EU RoHS compliant

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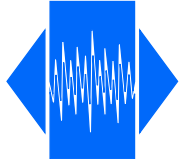
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From design to production
in Switzerland



QuartzCom AG reserves the right to make spec changes to this product



Handling Recommendation for SMD Crystal & Crystal Oscillator

1. ESD Handling

Crystal oscillators are electrostatic sensitive device. Therefore, direct touching of the terminals with fingers and without ESD precautions must be avoid.

Proper handling must be made according to the established ESD handling rules

IEC 61340-5-1 and EN 100015-1 to avoid degradations of the oscillator performance due to damages of the internal circuitry by electrostatic discharge.

2. Shocks & Vibrations

Excessive mechanical shocks and or vibrations during handling as well as manual and automatic assembly must be avoided.

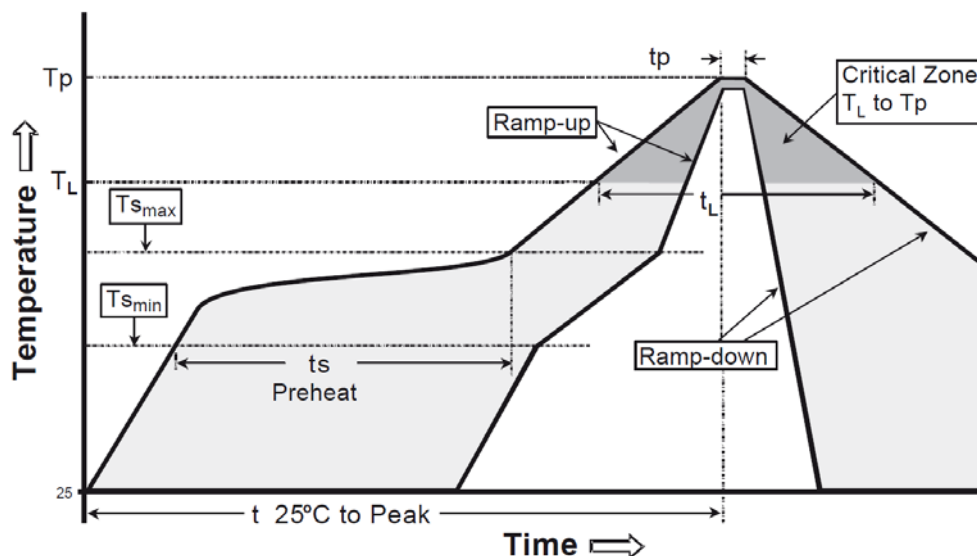
If accidentally, the component was dropped or subject to strong shock, component should be verified that the electrical function is still within the specification and still hermetically sealed.

3. Thermal Shocks

Avoid steep temperature gradients. It might lead to breakage of the crystal blank
Infrared reflow processes in general are safe.

4. Soldering & Cleaning

Reflow Condition in accordance with JEDEC STD-020C



Avoid washing or welding processes using Ultrasonic energy. These processes can damage the crystal due to mechanical resonance of the crystal blanks.

5. Coating

Using resin may have an impact on the oscillator characteristics.

If resin is used, please contact QuartzCom or our representative for more information.

In situations where resin would be used without contacting us in advance,

QuartzCom will not be responsible for any damages caused to the components or and injuries caused to people.

