

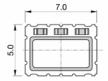


High reliable, accurate,

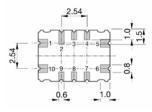
analogue temperature compensated (VC)TCXO

Generic specification

Frequency range	5.000 ~ 70.000 MHz				
Standard frequencies (fundamental)	5, 10, 12, 12.8, 13, 15.36, 16, 16.384, 19.2, 19.44, 20 25, 26, 30.72, 32, 40, 50 and 70 MHz				
Frequency stability:					
vs. temperature referenced to (Fмах+Fмім)/2	$\leq \pm 0.50 \text{ ppm}$	over -40 to +85 °C	(*)		
vs. supply voltage changes referenced to frequency at nominal supply	≤ ±0.1 ppm	±5 %			
vs. load changes referenced to frequency at nominal load	≤ ±0.1 ppm	±5 %			
vs. aging @ +40 °C	≤ ±1.0 ppm	1 st year			
G-sensitivity	2.0 ppb/g	per axis			
Frequency tolerance ex. factory	0 ~ +1.0 ppm @ +25 °C				
Supply voltage (nominal value ±5 %)	+2.5 V ~ +3.3 V (*		(*)		
Output signal	Clipped sine wave	CMOS	(*)		
Output level	> 0.8 Vp-p	$V_{OH} > 0.9*Vcc / V_{OL} < 0.$	1*Vcc		
Output load	10 kΩ // 10 pF	15 pF Max.			
Current consumption, depending on frequency	5 < mA	< 8 mA			
Electronic Frequency Control (EFC)	$\Delta F = \pm 5$ to ± 10 ppm	positive slope	(*)		
Control voltage (Vc)	+1.50 V ±1.0 V		(*)		
EFC input impedance	> 100 kΩ				
Tri-state function	pin #9 ➔ high or open pin #9 ➔ low or GND	pin #6 \rightarrow oscillation pin #6 \rightarrow high impedance	!		
Phase noise (typical value for 40 MHz)	-90 dBc/Hz -118 dBc/Hz -140 dBc/Hz -151 dBc/Hz -156 dBc/Hz	 @ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz @ 100 kHz 			
Operating temperature range	-40 ~ +85 °C		(*)		
Storage temperature range	-55 ~ +105 °C				
Reflow Profiles as per IPC/JEDEC J-STD-020C	\leq 260 °C over 10 sec. Max.				
Moisture sensitivity	Level 1 (unlimited)				





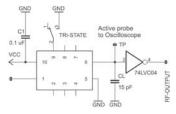


Pin function

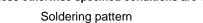
- Vc (EFC) for VC-TCXO GND or NC for TCXO # 1
- # 5 GND Output # 6
- # 9 E/D or NC
- # 10 Vcc

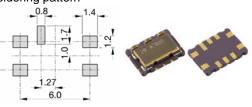
Do not contact #2, #3, #4, #7 & #8

Test circuit for CMOS

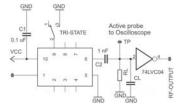


E-Mail





Test circuit for Clipped Sine Wave



2011/65/EU RoHS compliant

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From design to production

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in Switzerland





High reliable, accurate, analogue temperature compensated (VC)TCXO

Generic specification

Ordering code

(0)7S-(1)(2)-(3)(4)-(5)-40.000MHz		Example: VT7S-C33-NNu50-V10-40.000MHz		
(1) Output signal	(2) Supply voltage	(5) Pulling range		
H = CMOS	25 = 2.5 V	(VT only)		
C= Clipped sine wave	30 = 3.0 V	V05 = 1.5 ± 1.0 V ±5 ppm		
	33 = 3.3 V	V10 = 1.5 ± 1.0 V ±10 ppm		
(4) Frequency stability		W05 = 1.65 ± 1.0 V ±5 ppm W10 = 1.65 ± 1.0 V ±10 ppm		
$u25 = \pm 0.25 \text{ ppm}$				
$u50 = \pm 0.50 \text{ ppm}$ 1 $u0 = \pm 1.00 \text{ ppm}$ 1 $u5 = \pm 1.50 \text{ ppm}$		Z = special spec		
	(1) Output signal H = CMOS C = Clipped sine wave (4) Frequency stability $u25 = \pm 0.25 \text{ ppm}$ $u50 = \pm 0.50 \text{ ppm}$ $1u0 = \pm 1.00 \text{ ppm}$	(1) Output signal(2) Supply voltage $H = CMOS$ $25 = 2.5 V$ $C = Clipped sine wave$ $30 = 3.0 V$ $33 = 3.3 V$ $33 = 3.3 V$ (4) Frequency stability $u25 = \pm 0.25 \text{ ppm}$ $u50 = \pm 0.50 \text{ ppm}$ $1u0 = \pm 1.00 \text{ ppm}$		

Frequency stability vs. temperature

ppm	≤± 0.25	≤± 0.50	≤± 1.00	≤± 1.50
-20 to +70 °C	0	0	0	0
-40 to +85 °C	0	0	0	0
-40 to +95 °C	Δ	Δ	Δ	0
-40 to +105 °C	Х	Δ	Δ	Δ
-55 to +85 °C	Х	Δ	Δ	Δ

Δ Ask factory
O Available
X Not available

Environmental conditions

Test	IEC 60068 Part	IEC 60679-1 Clause	MIL-STD- 202G Method	MIL-STD- 810F Method	MIL-PRF- 55310D Clause	Test conditions (IEC)
Sealing tests (if applicable)	2-17	5.6.2	112E		3.6.1.2	Gross leak: Test Qc, Fine leak: Test Qk
Solderability Resistance to soldering heat	2-20 2-58	5.6.3	208H 210F		3.6.52 3.6.48	Test Ta method 1, Test Td₁ method 2, Test Td₂ method 2
Shock *	2-27	5.6.8	213B Cond C	516.4	3.6.40	Test Ea, 3 x per axis 100 g, 6 ms half-sine pulse
Vibration, sinusoidal*	2-6	5.6.7.1	204D Cond A	516.4-4	3.6.38.1 3.6.38.2	Test Fc, 30 min per axis, 10 Hz – 55 Hz 0,75 mm; 55 Hz – 2 kHz, 10 g
Vibration, random*	2-64	5.6.7.3	214A	514.5	3.6.38.3 3.6.38.4	Test Fdb
Endurance tests - ageing - extended ageing Other environmental		5.7.1 5.7.2	108A		4.8.35	30 days @ 85 °C 1000 h, 2000 h, 8000 h @ 85 °C 28 Dec. 20

Other environmental conditions on request

28 Dec. 20

2011/65/EU RoHS compliant

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VTX7S



High reliable, accurate, analogue temperature compensated (VC)TCXO

Generic specification

Handling Recommendation for SMD Crystal & Crystal Oscillator

1. ESD Handling

Crystal oscillators are electrostatic sensitive device. Therefore, direct touching of the terminals with fingers and without ESD precautions must be avoid.

Proper handling must be made according to the established ESD handling rules IEC 61340-5-1 and EN 100015-1 to avoid degradations of the oscillator performance due to damages of the internal circuitry by electrostatic discharge.

2. Shocks & Vibrations

Excessive mechanical shocks and or vibrations during handling as well as manual and automatic assembly must be avoided.

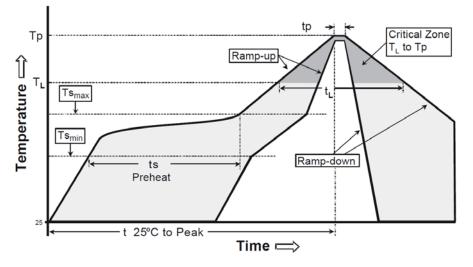
If accidently, the component was dropped or subject to strong shock, component should be verified that the electrical function is still within the specification and still hermetically sealed.

3. Thermal Shocks

Avoid steep temperature gradients. It might lead to breakage of the crystal blank Infrared reflow processes in general are safe.

4. Soldering & Cleaning

Maximum Reflow Condition in accordance with JEDEC STD-020C



Avoid washing or welding processes using Ultrasonic energy. These processes can damage the crystal due to mechanical resonance of the crystal blanks.

5. Coating

Using resin may have an impact on the oscillator characteristics. If resin is used, please contact QuartzCom or our representative for more information. In situations where resin would be used without contacting us in advance, QuartzCom will not be responsible for any damages caused to the components or and injuries caused to people.

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